

Shashank Obla

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Computer architecture researcher with comprehensive **cross-stack experience**, from custom digital tapeouts to datacenter-scale stochastic modeling and machine learning. Specialized in the design and optimization of **heterogeneous reconfigurable systems** across **networking, security, and database analytics** workloads.

EDUCATION

Carnegie Mellon University, Pittsburgh	2019 - 2026 (<i>Expected</i>)
Ph.D. Candidate, Electrical and Computer Engineering; GPA: 3.97/4.0 <i>PhD Thesis</i> : Design and Optimization of Input-Dependent Streaming Pipelines on FPGAs <i>Advisor</i> : Prof. James C. Hoe	
Indian Institute of Technology, Bombay	2014 - 2019
B.Tech and M.Tech, Electrical Engineering; GPA: 9.84/10.0 Minor in Biosciences and Bioengineering; GPA: 10.0/10.0 <i>Thesis</i> : Accelerated Circuit Simulation [thesis][paper] — <i>Advisor</i> : Prof. Sachin Patkar	

AWARDS

3rd Place Winner of Reconfigurable Computing Challenge at FCCM	May 2026
Institute Gold Medal – Indian Institute of Technology, Bombay	2019
Carnegie Institute of Technology Dean's Fellowship	2019

WORK EXPERIENCE

Intel Corporation	Summer 2020
<i>Programmable Solutions Group</i> — <i>Mentor</i> : Scott Weber	
- Modeled Partial Reconfiguration (PR) flows for next-generation FPGAs using SystemC to achieve sub-ms reconfiguration times utilizing existing hardware resources and to assess the benefits of new architectural decisions - Analyzed the full-stack implications of novel PR features by collaborating with cross-functional design teams	

RESEARCH EXPERIENCE

*preprint available

RapidQ: Queuing Abstraction and Tuning for Streaming Pipelines on FPGAs*	2022 - Present
- Designed the RapidQ abstraction for performance modeling of input-dependent streaming pipelines on FPGAs - Devised a modeling framework to extract the model directly from HLS implementations with over 97% accuracy - Engineered a queueing-based RapidQ simulator in SystemC achieving over 7x speedup over state-of-the-art Reduced resource utilization by over 40% across synthetic as well as real-world network security and machine learning workloads by developing an automated tuning flow powered by RapidQ	
RapidDetect: Threat Detection via FPGA-Accelerated Log Analysis* [paper][code]	2024 - Present
- Developed a heterogeneous FPGA-CPU pipeline for streaming log monitoring using Sigma rules at over 200Gbps - Implemented a highly-parameterizable string matching engine in HLS, tunable for line rates and log characteristics - Achieved a 100x reduction in threat detection latency and reduced costs by over 10,000x compared to commercial alternatives using a single FPGA server by integrating the FPGA string-matching filter with Hyperscan	
Group-by Aggregation Accelerator with NoC-enabled Partitioning	2025 - Present
- Architected a streaming group-by aggregation pipeline capable of processing over 64GBps on a single FPGA - Designed and open-sourced a parameterizable Network-on-Chip in RTL operating at over 500MHz, which has been used for hash-based tuple partitioning and also in the development of the NoC-based OpenFPGA by other groups - Reduced bandwidth by over 2x for skewed workloads with hot keys by introducing a fully-associative pre-aggregator	

SELECTED PUBLICATIONS

Conference Proceedings

- [Shashank Obla](#), Bin Li, James C. Hoe. “RapidQ: Queueing-based Performance Modeling Framework for Rapid Simulation and Automated Tuning of Input-Dependent Streaming FPGA Pipelines.” *Under Review*.
- [Shashank Obla](#), Tommy Tracy II, Matthew Beck, James C. Hoe, Kevin Skadron, Wajih Ul Hassan. “RapidScan: High-Throughput Parameterized HLS-based Streaming String Matching Library for FPGAs.” *Reconfigurable Computing Challenge, The 34th IEEE International Symposium on Field-Programmable Custom Computing Machines*, May 2026.
- Zhipeng Zhao, Joseph Melber, Siddharth Sahay, [Shashank Obla](#), Eriko Nurvitadhi, James C. Hoe. “Exploiting the Common Case When Accelerating Input-Dependent Stream Processing by FPGA.” *IEEE Transactions on Computers*, May 2023.

Posters

- [Shashank Obla](#), Bin Li, James C. Hoe. “Lightweight Queueing Abstraction for Rapid Simulation and Automated Tuning of Input-Dependent Streaming Pipelines on FPGAs.” *The 34th IEEE International Symposium on Field-Programmable Custom Computing Machines*, May 2026.

TEACHING EXPERIENCE

Evidence Based Teaching in STEM

2024

Course offered by Eberly Center for Teaching Excellence & Educational Innovation at CMU

- Developed a new course including learning objectives-driven syllabus design and inquiry-based learning assignments
- Refined teaching skills through practice teaching sessions and critically reviewed Scholarship in Teaching and Learning

Performance Modeling Tools for Computer Systems Researchers

2022 (volunteer)

Graduate Teaching Assistant – Prof. Mor-Harchol Balter

- Mentored 20+ PhD students in **applying queuing theory** to their systems research through one-on-one meetings
- Designed homework assignments to enable students to develop and verify insights through queuing system simulations

Reconfigurable Logic: Technology, Architecture, and Applications

2020, 2021, 2022 (volunteer)

Graduate Teaching Assistant – Prof. James C. Hoe

- Developed a DFX-capable Vitis platform for Ultra96v2 enabling students to gain first-hand experience in using role-and-shell partial reconfiguration in the lab exercises and in their course projects
- Redesigned the recitation syllabus and conducted recitations introducing system design concepts for FPGAs

OTHER PROJECTS

Accelerating Stencil Computation – Multigrid V-Cycle Poisson Solver [\[pdf\]](#)

2022

- Achieved **140x speedup** (over 50% of arithmetic peak) using **SIMD intrinsics** compared to [Proto](#) from LBNL

Enabling Design Tradeoffs at Runtime with Dynamic Composition – *ECE Qualifiers* [\[pdf\]](#)

2021

- Implemented a **hierarchical PR** architecture to dynamically tune modules to changing constraints and opportunities showcasing **3x improvement** in performance for a Breadth-First Search accelerator over static provisioning

FPGA Tape-Out in TSMC 28nm — *Course Project funded by Apple*

2020

- Designed, taped out and post-silicon verified a **custom FPGA fabric** supported by the VTR software toolchain

SERVICE AND LEADERSHIP

Student Council for Faculty Hiring – CMU ECE

2023 - 2024

- Chaired the first such student council at ECE, **managing** a group of **25 students** in conducting faculty **interviews**

TECHNICAL SKILLS

Programming	SystemVerilog, Vitis/Altera HLS, SystemC, C++, Assembly/SIMD Intrinsics, Python
Design Tools	Quartus, Vivado, Platform Architect, Verilog-to-Routing, Cadence Genus/Innovus/Virtuoso/Voltus
Research Areas	FPGAs, Computer Architecture, Digital Design, High-Performance Computing, Queuing Theory